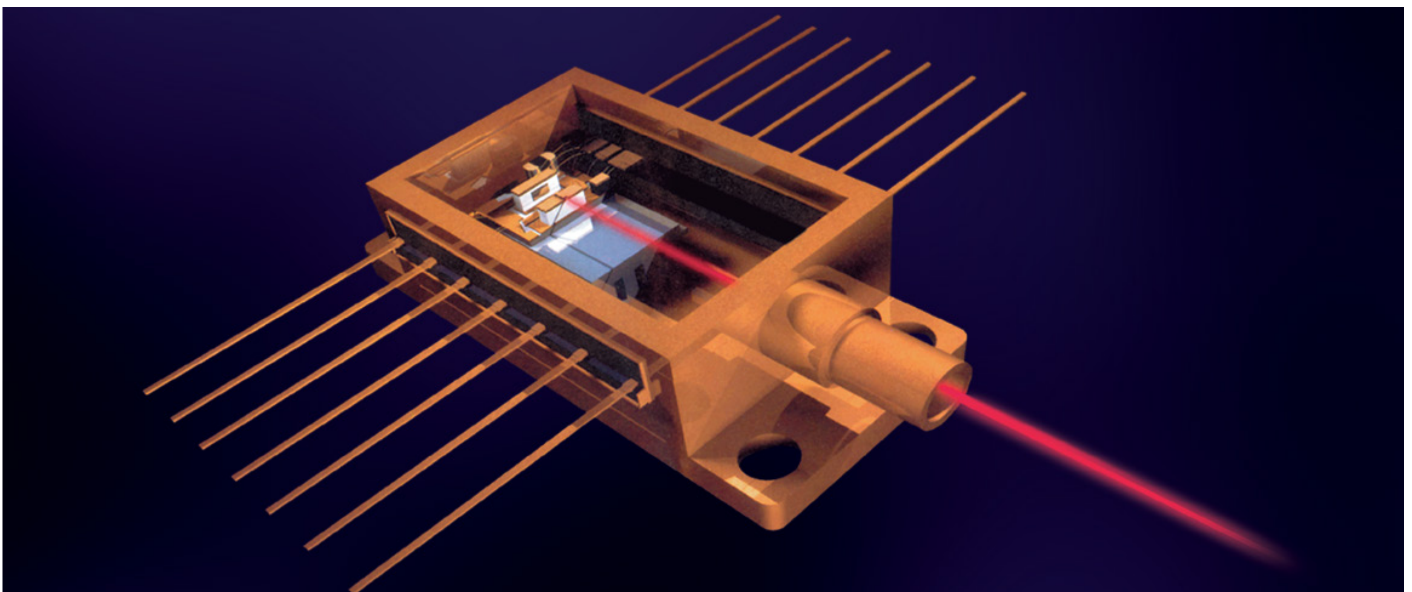
RELIABILITY AND LIFETIME CONSIDERATIONS FOR HIGH STABILITY GOLD TERMINATED NTC CHIP THERMISTOR



RELIABILITY DATA AND LIFETIME MODELLING OF TE CONNECTIVITY NTC CHIP THERMISTORS (LEADLESS, GOLD-TERMINATED CHIPS) FOR APPLICATIONS IN TELECOMMUNICATIONS AND OPTOELECTRONICS, BASED ON GENERAL PRINCIPLES OF TELCORDIA SR-332.

As the global demand for telecommunications connectivity and systems continues to grow there is an expectation that the overall performance of those systems will be enhanced. Consideration of performance includes factors such as network speed, bandwidth, storage capacity and reliability.

System reliability can be defined as the ability of a system to perform specified functions for specified time intervals under specified operating conditions, without failure.

System reliability depends on the reliability of the modules and components that comprise the system. Reliability can be defined and quantified so that it is an important design factor to be considered in system development. This paper discusses some reliability and lifetime considerations for particular types of electronic components: Negative Temperature Coefficient (NTC) Thermistors.

NTC Thermistor components are formed from ceramic materials that have semiconductor properties. This means that the number of charge carriers available for electrical conduction increases as temperature increases so that electrical resistance decreases as temperature increases. This effect is described by a Negative Temperature Coefficient of Resistance, and the components are classified as "NTC Thermistors" or Thermally Sensitive Resistors. The use of NTC Thermistors as Temperature Sensors is based on a defined relationship between Resistance and Temperature, the R/T characteristics.

This is defined by the Steinhart-Hart Equation which is a relationship of the form:

$$T(°C) = \left(\left(\frac{1}{A + (B \times ln(R)) + (C \times (\ln(R))^3)}\right) - 273.15\right) \qquad (1)$$

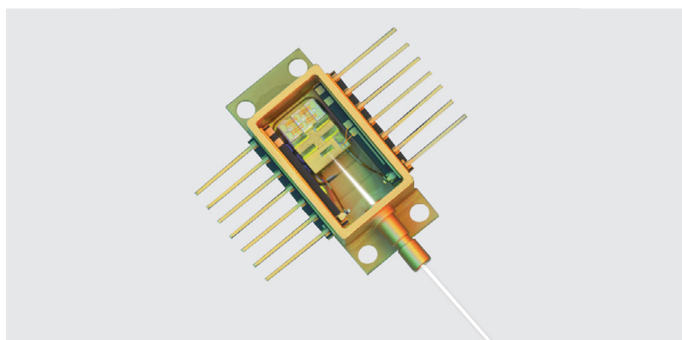
Where T is the Temperature in degrees Centigrade, R the Resistance in Ohms, and A, B and C are constants derived from Resistance/Temperature calibrations.

NTC Thermistors are used extensively for Temperature Sensing in various applications in telecommunications and optoelectronics modules. The typical physical form of the NTC sensors used in such applications is a chip, with dimensions of the order of 0.35 to 1mm in length and width and thickness of the order of 0.20 to 0.75mm.

There is conductive metallisation on opposing faces so that conduction is through the chip. Gold is typically used as a conductor material to optimise thermal and electrical conduction and to be compatible with wire-bonding and die-attach technology.

A typical mounting arrangement for Gold Chip thermistors is as shown below:

SEM PHOTO 30X HYBRID THERMISTOR CHIP



TYPICAL APPLICATION FOR GOLD TERMINATED NTC CHIP, LASER DIODE PACKAGE

The essential reliability consideration for NTC Thermistors is that the R/T characteristics conform to defined tolerance limits.

NTC thermistors rarely fail in a catastrophic manner. Rather than failing through open-circuit or short circuit behaviour they show a change or drift in resistance. A value of ± 1.0% change in resistance value at 25°C is used as a typical limit for practical situations, but different limits may be applied depending on the application.

Reliability Definitions and Parameters:

The failure rate for components is usually designated as λ and is generally expressed as "failures per unit time", typically failures per hour, λ_{hours}.

An associated value used to describe reliability of components is Mean Time to Failure, referred to as MTTF and usually designated as θ. MTTF is the reciprocal of the failure rate so that:

$$MTTF_{hours} = {}^{1}/_{\lambda_{hours}} \quad (2)$$

$$MTTF_{years} = {}^{1}/_{(\lambda_{hours} \times 24 \times 365)} \quad (3)$$

Because the number of failures per hour is generally very low, the electronics component and semiconductor industries also describe failure rate in terms of "Failures in Time" or FIT which is defined as the failure rate per billion hours so that:

$$FIT = \lambda_{FIT} = \lambda_{hours} \times 10^9 \quad (4)$$

Reliability modelling and predictions are based on components operating in normal lifetime conditions where the failure rate is approximately constant. In this situation the distribution of failures as a function of time is of the form:

$$f(t) = \lambda e^{-\lambda t} \quad (5)$$

It is usually not practical to make extensive measurements of failure rates in actual applications under normal operating conditions. Instead, the principle of Highly Accelerated Stress Testing (HAST), is used to measure failure rates at elevated stress levels. Extrapolation calculations are then performed to predict failure rates at normal operating conditions.

For NTC Thermistor components the relevant failure mode is a change in resistance at a reference Temperature, relative to defined limits. This failure mode is due to various failure mechanisms, such as propagation of micro-cracks in the ceramic material and changes at the interface between the metallization and the ceramic material. The main stress that influences the development of failure modes is the temperature to which components are exposed so temperature stress testing is considered here.

The rate at which the observed failure mode progresses can be modelled mathematically by the Arrhenius Rate Equation which states:

$$R \propto e^{\frac{-Ea}{kT}} \quad (6)$$

Where R is the rate of progression of the failure mode, e = 2.7183, (base of Natural Logarithms) k is Boltzmann's Constant: 8.6x10^{-5} eV/K (electron-Volt per Kelvin). T is the Temperature in Kelvin, Ea is the Activation Energy, expressed in electron-Volt which is estimated from evaluations and proprietary data for NTC Thermistors.

For most practical situations, for NTC Thermistor components at temperatures in the approximate range -40°C to +200°C, the value of Ea is approximately constant so the relative rate of progression of the failure mode is dependent on temperature.

It is useful to define an acceleration factor, designated as A_f, which is the ratio of the rates of failure mode progression for a component at two different temperatures. When the normal operating temperature is designated as T_{use} and the elevated temperature used for stress testing is designated as T_{test}, and the associated rates as R_{use} and R_{test}, then the Ratio and the Acceleration Factor are given by:

$$\frac{R_{test}}{R_{use}} = A_f = e^{\frac{Ea}{k}\left(\frac{1}{T_{use}} - \frac{1}{T_{test}}\right)} \quad (7)$$

The acceleration factor is used to develop a High Temperature Operating Life (HTOL) model.

In this model the failure rate, λ, for a sample of components is defined as the ratio of the total number of failures and the cumulative time of operation which is defined as Equivalent Device Hours (EDH), with

$$EDH = D \times H \times A_f \quad (8)$$

where: D = Number of devices tested
H = Test hours per device
Af = Acceleration Factor derived from the Arrhenius equation

The failure rate per hour, λ_{hours} is then given by:

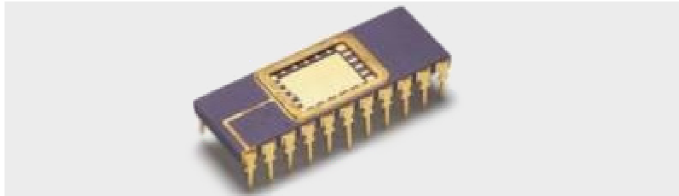
$$\lambda_{hours} = \frac{r}{EDH} \quad (9)$$

Where r is the number of failures observed in the sample for which the EDH value was defined.

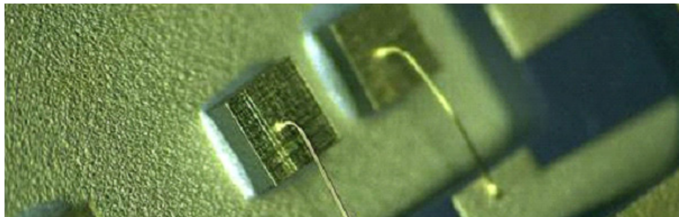
In practice, the term r, is defined by applying a probability function (χ^2, Chi-squared) to the observed number of failures to model their statistical distribution in the relevant time interval.

Evaluations and Results:

These principles were used in evaluations at TE Connectivity to derive values for failure rates and Mean Times To Failure (MTTF) for variants of electro-ceramic material systems used to produce Gold Chip NTC Thermistor Components. Samples of each variant were mounted in 20-pin CerDIP packages, using silver filled epoxy to form a mechanical, thermal and electrical bond to the substrate and with a gold wire bond to the top electrode as shown:



CERDIP PACKAGE USED FOR MOUNTING GOLD TERMINATED NTC CHIP DURING EXTENDED LIFE-TESTING



MAGNIFIED VIEW OF GOLD TERMINATED NTC CHIP MOUNTED FOR EXTENDED LIFE-TESTING

The components were subjected to Accelerated Stress Testing and evaluations were performed based on principles outlined in Telcordia SR-332.

After an initial screening of the components, calibrations were performed on a test fixture in an oil bath at +25°C ±0.05°C at zero-power conditions. The thermistors in the CerDIP packages were subjected to un-powered temperature stress, in air, at "stress test" temperatures of +50°C, +75°C, +100°C, +125°C, +150°C.

For each electro-ceramic material type, statistically significant numbers of samples were used for evaluations at these temperatures with calibrations at +25°C performed at 0 hours as reference and after stress test intervals of 336 hours, 1008 hours, 2016 hours, 7560 hours and 10080 hours.

These calibration intervals and values were used to calculate values for cumulative Equivalent Device Hours (EDH) and failure rates relative to various resistance drift limits based on the initial resistance values at 25°C.

The results of the evaluations can be summarised as follows:

TE Connectivity Electro-Ceramic Material System	Beta Value β(25-85) (K)	MTTF for ±1% ΔR at +30°C Operating Temperature (Years)	Typical Range of Chip Resistance Values at +25°C (kΩ)	Nominal Ohmic Value at +25°C used for Dimension Calculation (kΩ)	Typical Chip Dimensions [Length x Width] (mm)
BT4-D	3694	365	5 to 30	10	0.92 x 0.92
BT3-D	3976	106	2 to 20	10	1.00 x 1.00
BT3Lo-D	3978	66	2 to 10	10	0.44 x 0.44
BT647-D	3956	115	2 to 15	10	0.60 x 0.60
BT647H-D	3956	361	2 to 15	10	0.55 x 0.55
BT647H-H	3956	88	2 to 15	10	0.36 x 0.36
BT6-D	4262	212	50 to 200	100	0.76 x 0.76
BT63-H	4075	72	50 to 200	100	0.37 x 0.37

TABLE 1: MTTF AND CHIP CONFIGURATION DATA FOR TE CONNECTIVITY ELECTRO-CERAMIC MATERIAL SYSTEMS

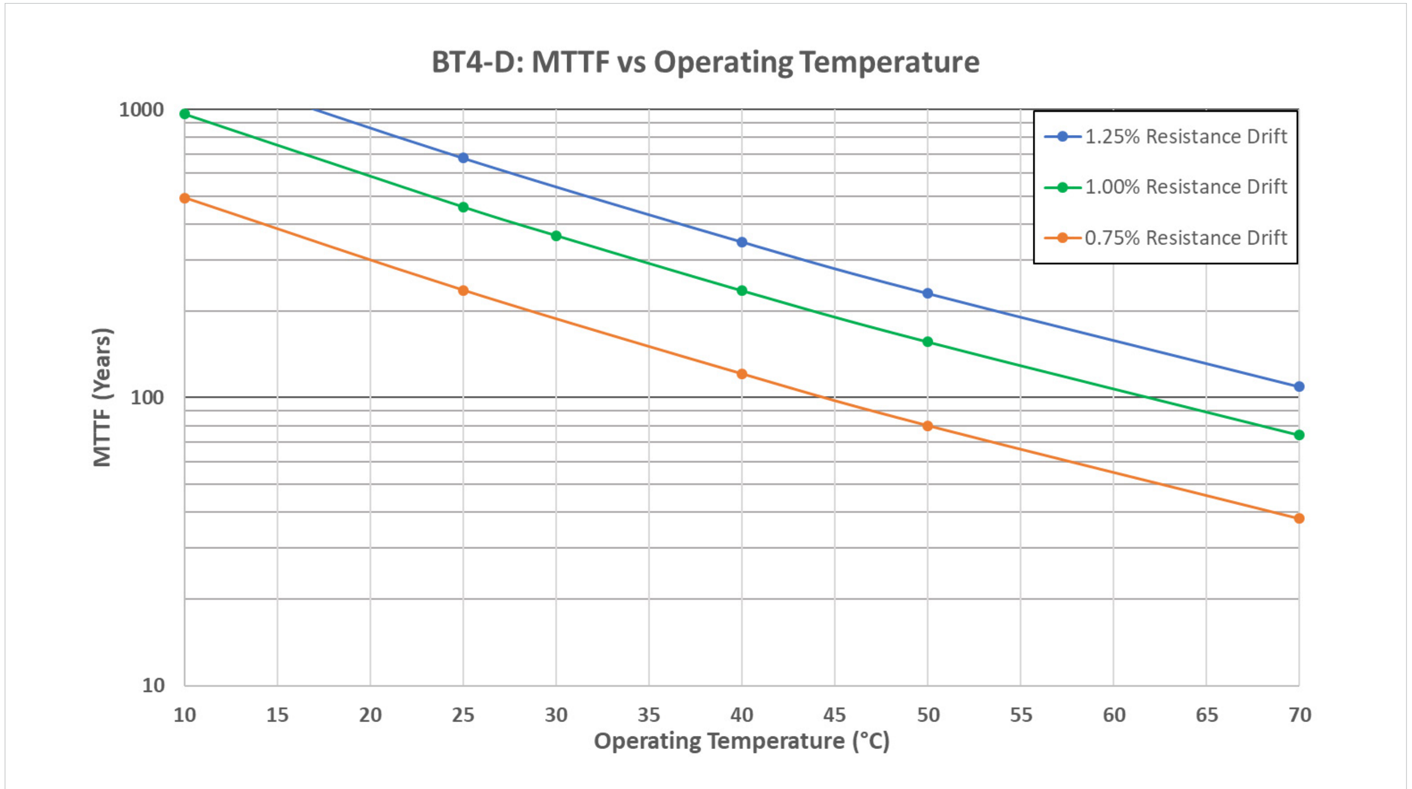


FIGURE 1: MTTF VS OPERATING TEMPERATURE FOR ELECTRO-CERAMIC MATERIAL SYSTEM BT4-D

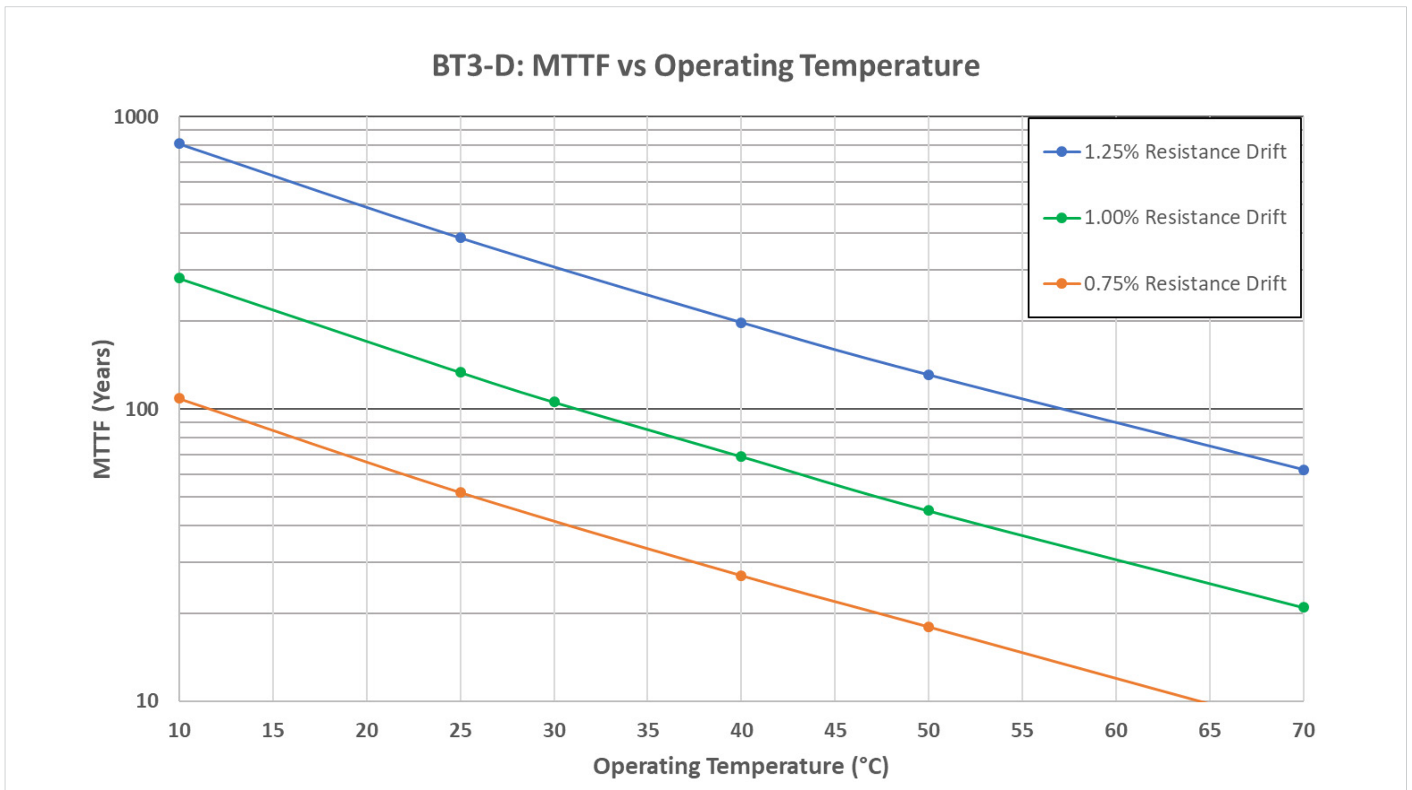


FIGURE 2: MTTF VS OPERATING TEMPERATURE FOR ELECTRO-CERAMIC MATERIAL SYSTEM BT3-D

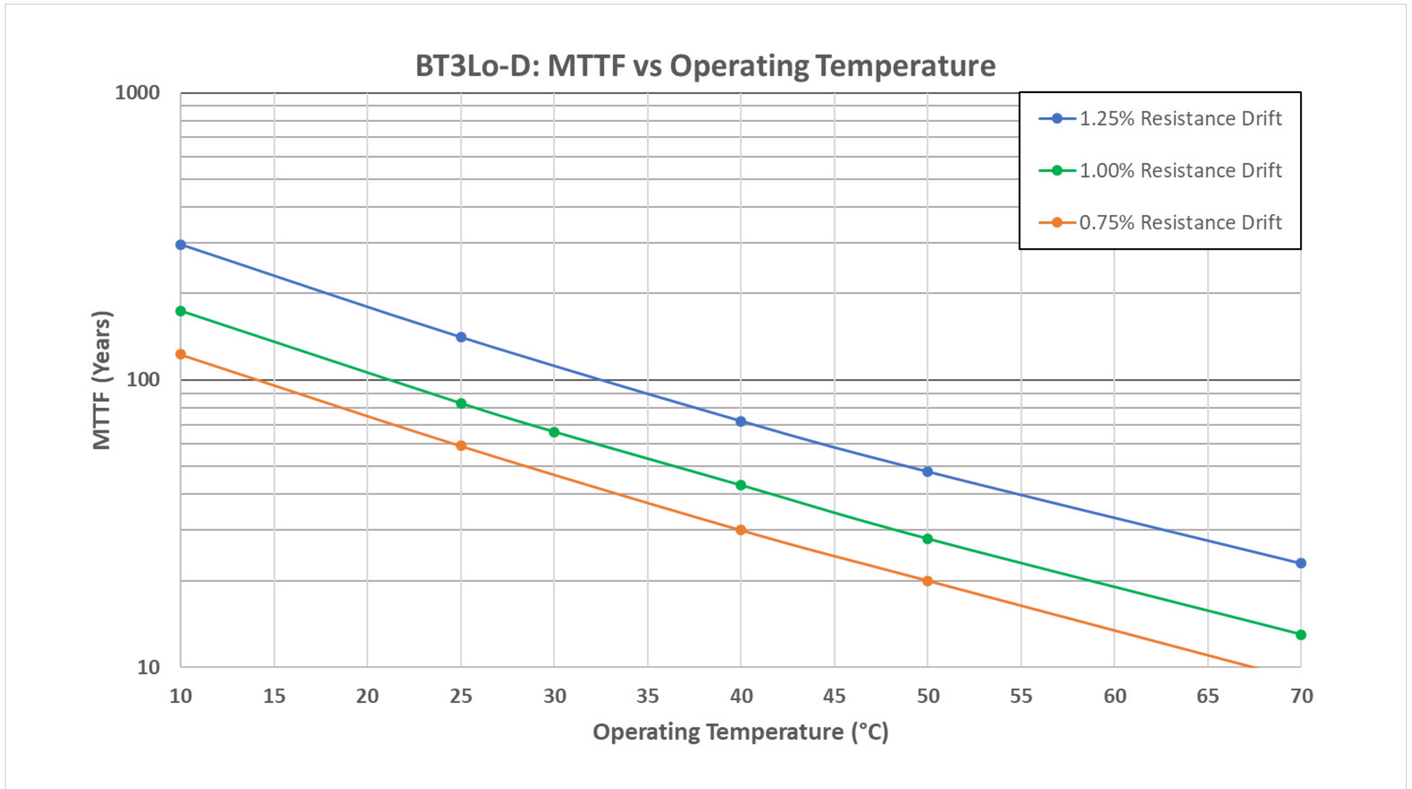


FIGURE 3: MTTF VS OPERATING TEMPERATURE FOR ELECTRO-CERAMIC MATERIAL SYSTEM BT3LO-D

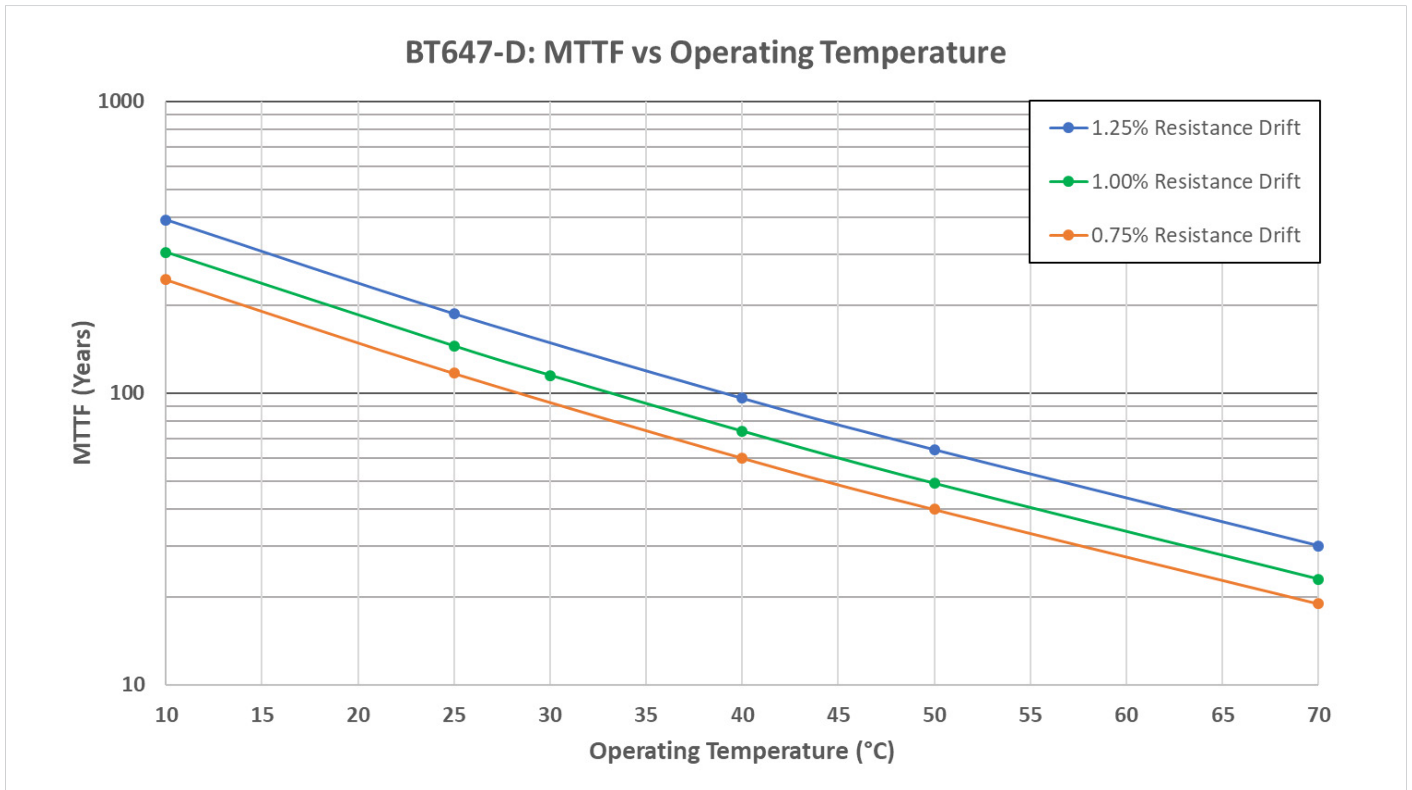


FIGURE 4: MTTF VS OPERATING TEMPERATURE FOR ELECTRO-CERAMIC MATERIAL SYSTEM BT647-D

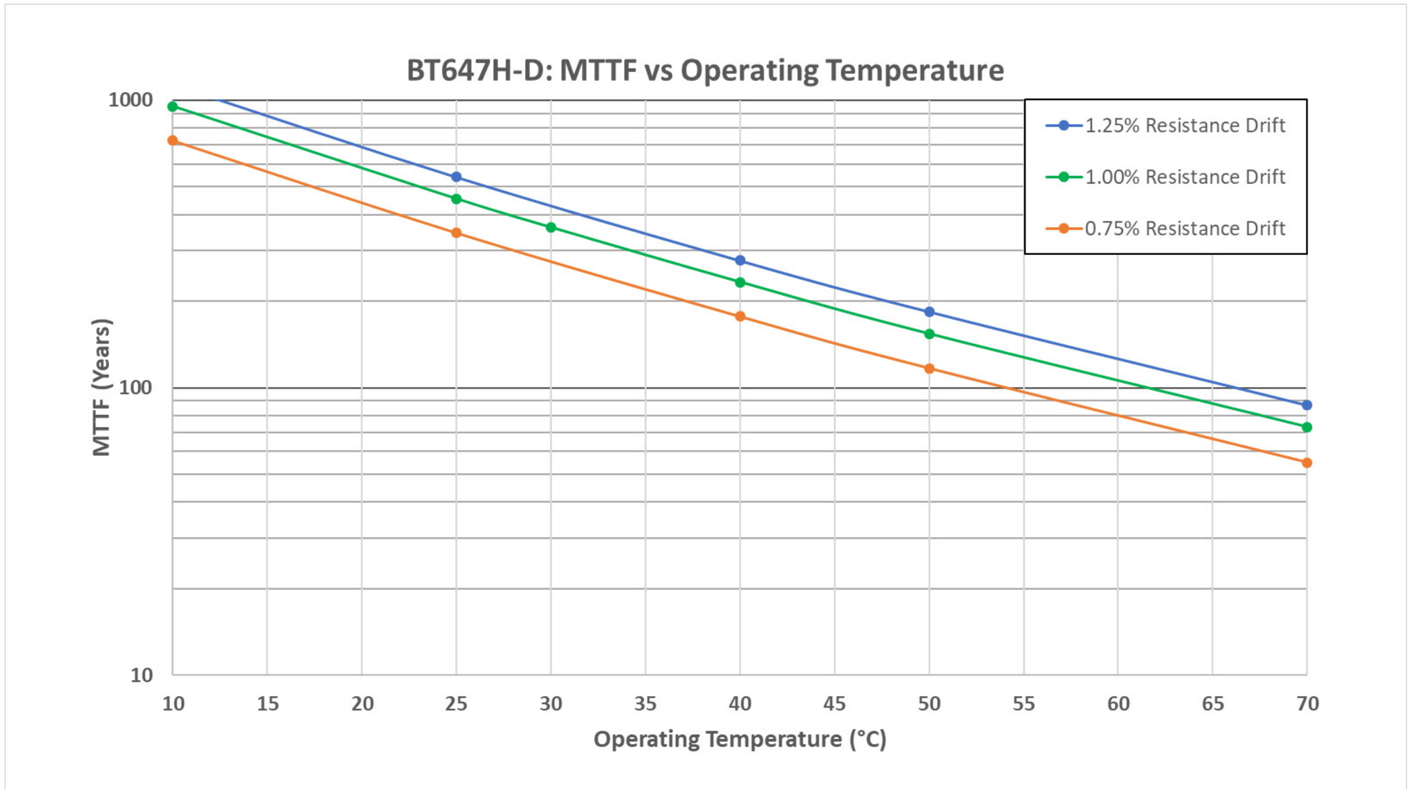


FIGURE 5: MTTF VS OPERATING TEMPERATURE FOR ELECTRO-CERAMIC MATERIAL SYSTEM BT647H-D

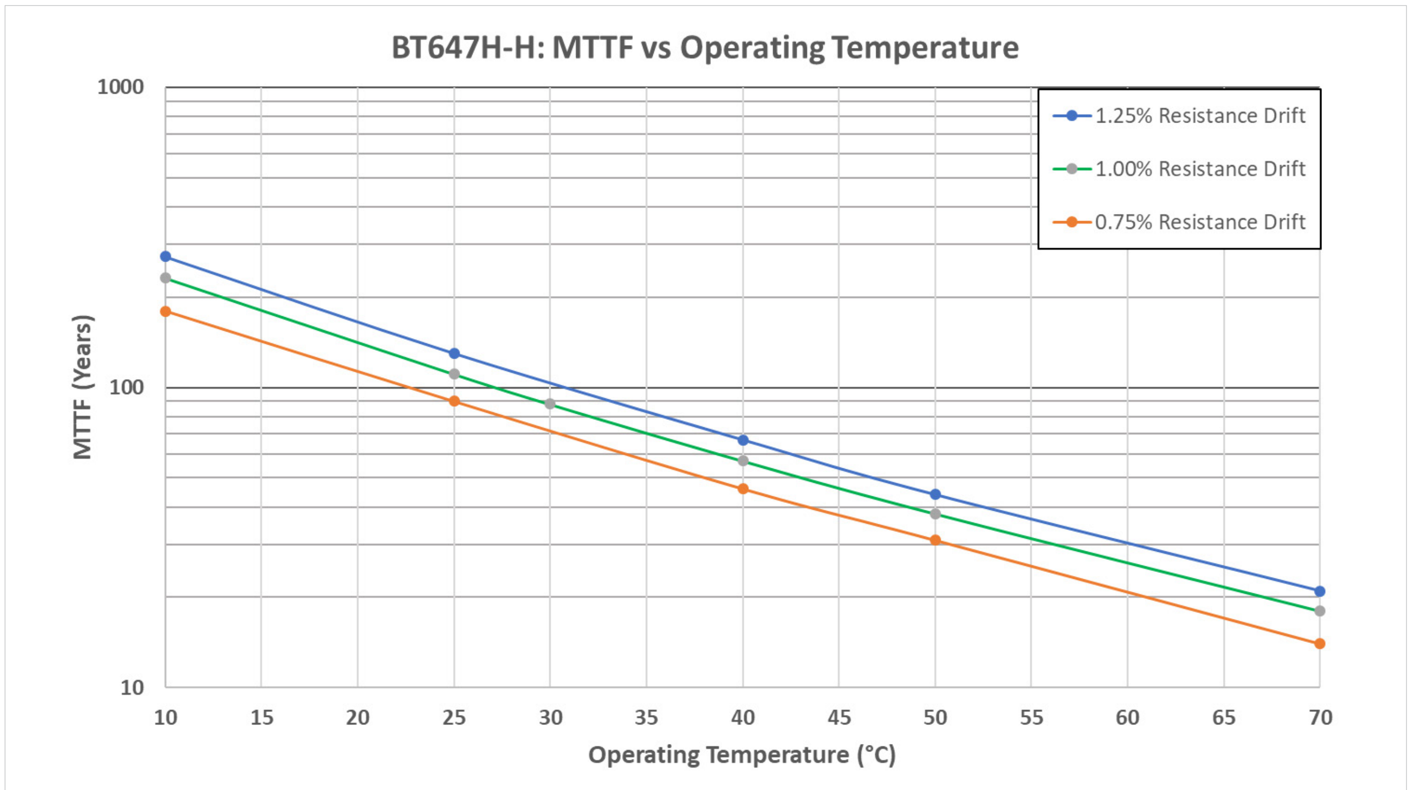


FIGURE 6: MTTF VS OPERATING TEMPERATURE FOR ELECTRO-CERAMIC MATERIAL SYSTEM BT647H-H

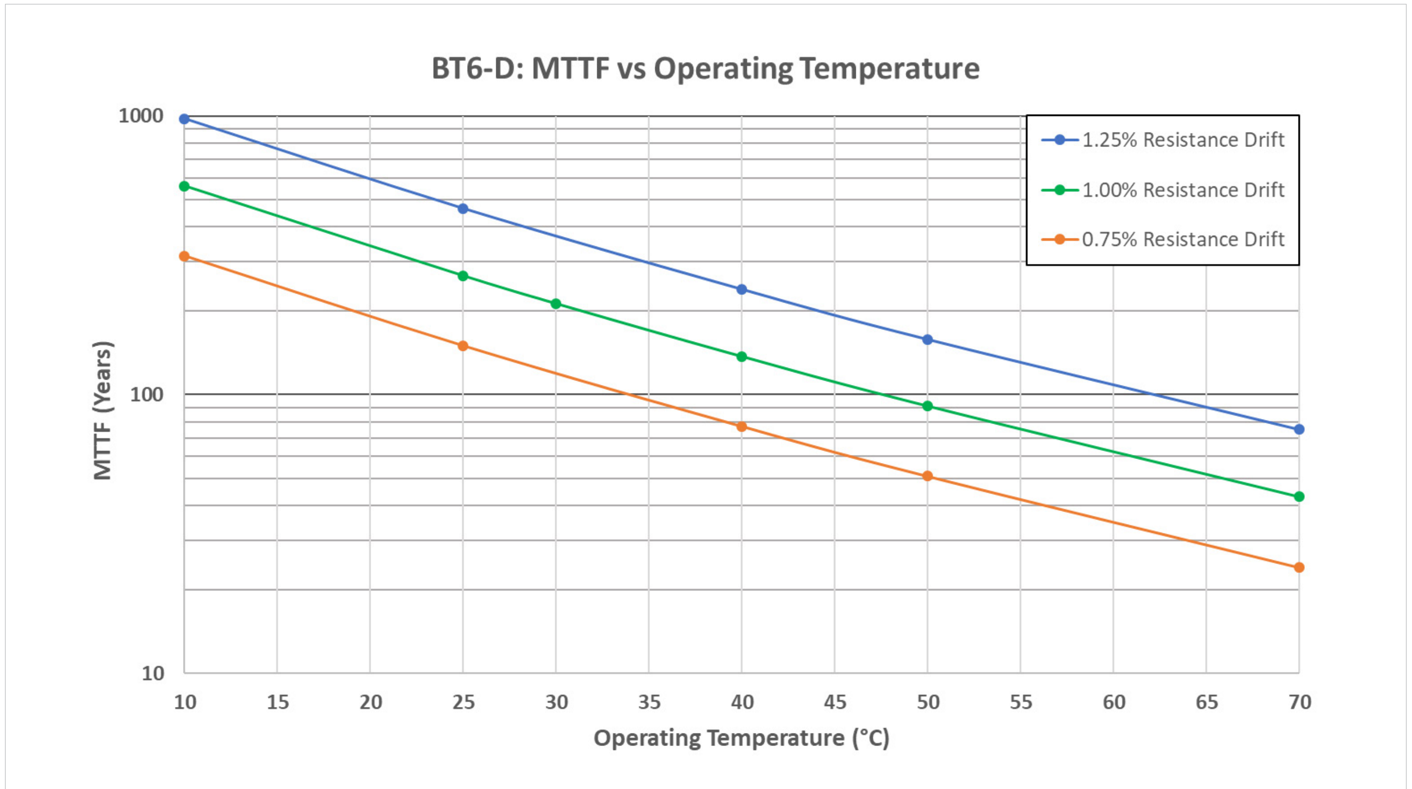


FIGURE 7: MTTF VS OPERATING TEMPERATURE FOR ELECTRO-CERAMIC MATERIAL SYSTEM BT6-D

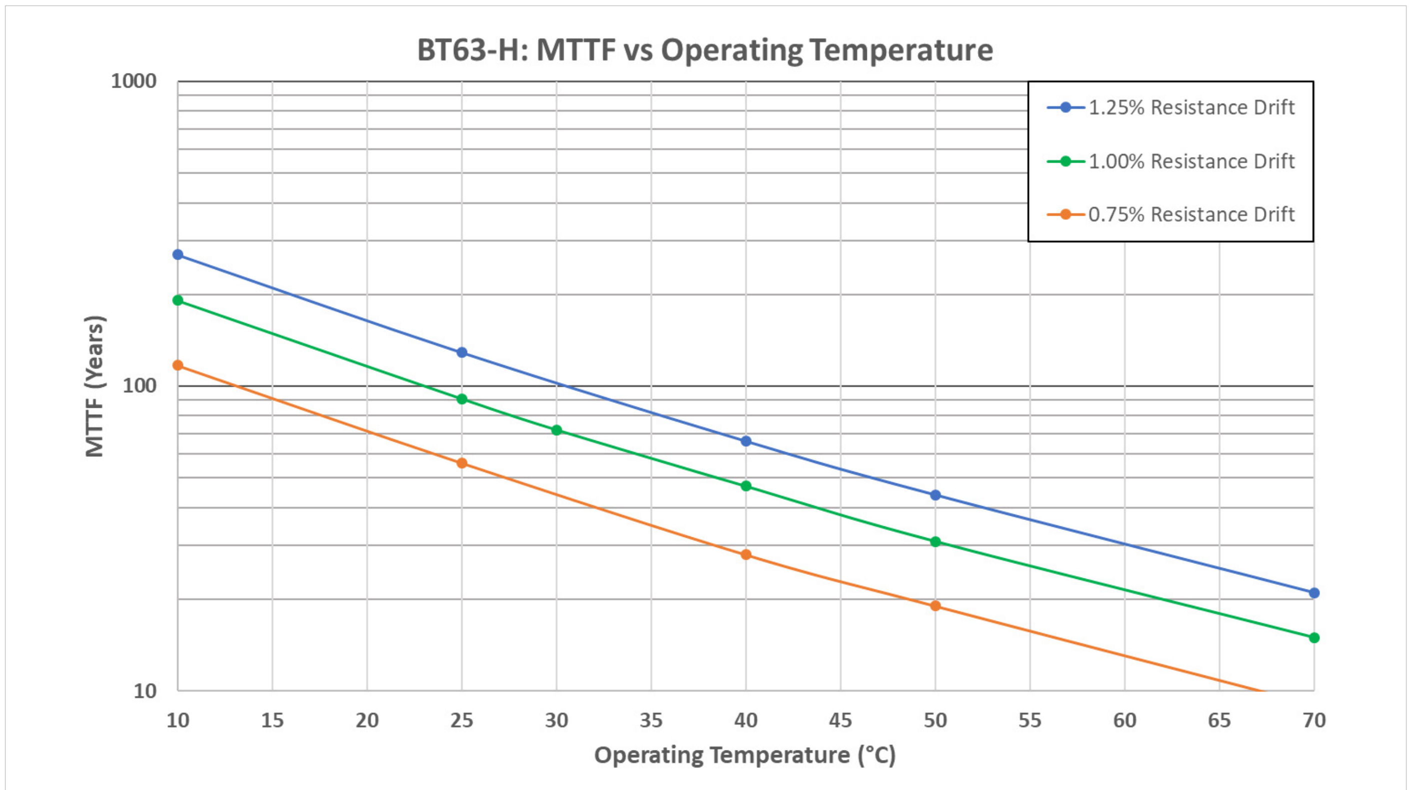


FIGURE 8: MTTF VS OPERATING TEMPERATURE FOR ELECTRO-CERAMIC MATERIAL SYSTEM BT63-H

Conclusions:

This paper has outlined some of the principles and considerations for generating extended reliability data for Gold Chip NTC thermistor materials using Accelerated Stress Testing based on the Arrhenius Equation and a High Temperature Operating Life Model (HTOL).

The presented data and analysis provide estimated values of Mean Time To Failure for Gold Chip NTC Thermistors using various electro-ceramic material systems. The information is intended to provide design engineers with an overview of some of the critical factors in physical form, Resistance/Temperature characteristics, and reliability considerations for optoelectronic system design.

The data provides confidence in the use of **TE Connectivity Gold Chip Thermistor** products in systems where the expected operating lifetime exceeds 20 years.

As the range of applications for Gold Chip Thermistors continues to develop it is advisable to perform reliability evaluations based on configurations that reflect actual operating conditions. TE Connectivity can provide technical support to optimise the performance of NTC Gold Chip sensors in systems which depend on accurate and reliable Temperature Measurement.

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